REMARKS

This Response is responsive to the final Office Action mailed April 22, 2008. Claims 1-6, 8, and 25-28 are pending. Claims 1, 6, 8, and 25-28 have been amended. Claim 10 has been cancelled. In view of the following remarks, as well as the preceding amendments, Applicants respectfully submit that all claims in this application are in complete condition for allowance and request reconsideration of the application in this regard.

Rejections of Claims Under 35 U.S.C. § 103

Claims 1-6, 8, 10, and 25-28 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Choi et al. (U.S. Patent No. 6,566,704), hereinafter *Choi*. Claims 1 and 23 are independent claims. Applicants respectfully disagree with this rejection for the reasons set forth below.

With regard to independent claim 1, the Examiner states that "Choi et al. do not explicitly state in the embodiment of figure 3F a plurality of semiconducting nanotubes." However, to support the rejection, the Examiner contends that:

> Choi et al. teach using a plurality of semiconducting nanotubes in the disclosed invention of nano sized transistor (see, for example, column 3, lines 39-43), wherein figures 1-3 depict only a unit cell of the transistor (column 3, lines 41-43). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a plurality of semiconducting nanotubes in Choi et al.'s device in order to use the device in a practical application which requires a plurality of semiconducting nanotubes, such as a nano sized transistor.

The general statements regarding the plural term "carbon nanotubes" made at column 3, lines 39-41 of *Choi* fail to support a conclusion that the unit cell shown in Figures 1-3 of *Choi* can be modified to include more than one semiconducting nanotube. In fact, the unit cell shown in each of Figures 1-3 of *Choi* is described as including a nano-sized hole (10') and a nanotube (100) with a nano-sized diameter. Hence, the dimensions of the hole (10') and the nanotube (100) are commensurate. *Choi* fails to disclose or suggest that the dimensions of the hole (10') can be increased to accommodate multiple semiconducting nanotubes (100). Hence, without more explanation, the general statements made at column 3, lines 39-41 of *Choi* do not

objectively lead to the conclusion that the unit cell shown in Figures 1-3 of *Choi* can be modified to include multiple semiconducting nanotubes. Hence, any conclusion by the Examiner that the unit cell shown in Figures 1-3 of *Choi* can include multiple semiconducting nanotubes is based solely upon the hindsight provided by Applicants' own specification.

In the absence of more information, the Examiner's argument that "to use the device in a practical application ... requires a plurality of semiconducting nanotubes" is believed by the Applicants to apply to the use of the unit cell shown in Figures 1-3 of *Choi* in a setting that includes multiple unit cells. Even if one were to replicate the single nanotube unit cell shown in Figures 1-3 of *Choi* to make multiple unit cells, each of the individual unit cells would still only include a single semiconducting nanotube. Applicants claim 1 sets forth that the device structure includes a plurality of semiconducting nanotubes.

Independent claim 1 sets forth that each semiconducting nanotube has "a channel region extending vertically through said gate electrode." Figures 4A and 4B of *Choi* contain the only unambiguous disclosure in *Choi* of a device structure having multiple nanotubes (100). However, *Choi* teaches that the gate electrode (20) and gate dielectric (30) are disposed in a layer stack above the nanotubes (100). Hence, were one to attempt to modify the device structure shown in Figure 3F of *Choi* based upon the only disclosure of multiple nanotubes (100) in *Choi* as shown in Figures 4A and 4B, the channel region of each of the nanotubes (100) would no longer extend vertically through the gate electrode (20), as set forth in Applicants' independent claim 1.

For at least these reasons, Applicants submit that the Examiner has failed to properly support a case of *prima facie* obviousness with regard to independent claim 1. Therefore, Applicants respectfully request that the Examiner withdraw this rejection.

Applicants' independent claim 25 is patentable for at least the same or similar reasons as claim 1. Because claims 2-6 and 8 depend from independent claim 1 and claims 26-28 depend from independent claim 25, Applicants submit that these claims are also patentable for at least the same reasons discussed above. Furthermore, these dependent claims recite unique combinations of elements not disclosed or suggested by *Choi*.

Conclusion

Applicants have made a bona fide effort to respond to each and every requirement set forth in the Office Action. In view of the foregoing remarks, this application is submitted to be in complete condition for allowance and, accordingly, a timely notice of allowance to this effect is earnestly solicited. In the event that any issues remain outstanding, the Examiner is invited to contact the undersigned to expedite issuance of this application.

Applicants do not believe fees are due in connection with filing this communication. If, however, any fees are necessary as a result of this communication, the Commissioner is hereby authorized to charge any under-payment or fees associated with this communication or credit any over-payment to Deposit Account No. 23-3000.

Respectfully submitted,

June 24, 2008
Date

/William R. Allen/
William R. Allen, Ph.D.
Reg. No. 48,389
WOOD, HERRON & EVANS, L.L.P.
2700 Carew Tower
441 Vine Street
Cincinnati, Ohio 45202
Telephone: (513) 241-2324
Facsimile: (513) 241-6234